REMARKS

The Office Action mailed December 11, 2006 has been received and reviewed. Claims 1-30 are pending. Claims 8, 19, and 29 stand rejected under 35 U.S.C. §112 second paragraph. Claims 1-30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Published Application No. 2004/0044833 by Ryan and U.S. Patent 5,502,621 to Schumacher. Claims 1-30 stand provisionally rejected on the ground of nonstatutory obviousness-type double patenting in view of copending Application Serial No. 11/417,389 in view of Ryan and Schumacher.

Rejections Under 35 U.S.C. §112

Claim 29 stands rejected as being indefinite for reciting the phrase "substantially parallel edges of the circuit board." Applicant respectfully asserts that the cited phrase is not indefinite. The word "substantially" has been interpreted by the Federal Circuit as meaning "largely but not wholly that which is specified." *Playtex Products, Inc. v. Procter & Gamble Co.*, 400 F.3d 901, 906 (Fed. Cir. 2005) The Federal Circuit has further held that "substantial" is not indefinite. *Liquid Dynamics,* 355 F.3d 1361, 1368 (Fed. Cir. 2004) ("The term 'substantial' is a meaningful modifier implying 'approximate' rather than 'perfect.'"); *Anchor Wall Systems, Inc. v. Rockwood Retaining Walls, Inc.*, 340 F.3d 1298, 1311 (Fed. Cir. 2003) ("[T]erms such as 'approach each other,' 'close to,' 'substantially equal,' and 'closely approximate' are ubiquitously used in patent claims and that such usages, when serving reasonably to describe the claimed subject matter to those of skill in the field of the invention and to distinguish the claimed subject matter from the prior art, have been accepted in patent examination and upheld by the courts").

The specification need not specify what is meant by words of approximation. In particular, the Federal Circuit has interpreted the phrase "generally parallel" to be sufficiently definite without any further definition:

> The written description does not specify any special definition for the terms 'generally,' 'parallel,' or the phrase 'generally parallel.' *See, e.g.,* 015 patent, col. 5, ll. 5-6 ('The top surface 26 generally lies parallel to the bottom surface 28.'); 713 patent, col. 5, ll. 10-11 (same). Moreover, nothing in the prosecution history of the 015 patent family clearly limits the scope of "generally parallel" such that the adverb "generally" does not broaden the meaning of parallel.

> Accordingly, we hold that the phrase 'generally parallel' envisions some amount of deviation from exactly parallel.

Anchor Wall Systems, Inc. v. Rockwood Retaining Walls, Inc., 340 F.3d 1298, 1311 (Fed. Cir. 2003)

Double Patenting Rejection

Claims 1-30 stands provisionally rejected under the judicially created doctrine of obviousness-type double patenting in view. Applicant respectfully asserts that an obviousness-type double patenting rejection is improper. As discussed below, the combination of Schumacher and Ryan is not suggested in the prior art and therefore the claims are not obvious in view of the claims of Ryan.

Discussion of the Disclosed Embodiment

The disclosed embodiments of the invention will now be discussed in comparison to the prior art. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the prior art subject matter, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

The application discloses embodiments in which pairs of memory devices are arranged surrounding a memory hub with each pair of memory devices being substantially perpendicular to adjacent pairs. Each memory device is coupled to the memory hub by a control-address bus and a data bus. The memory device has first and second ends with data pins located at one end and control-address pins at the other end. The first ends of the memory devices are positioned adjacent one another such that, for example, the data buses extending to the data pins of the memory devices are next to one another, which reduces skew and other defects. The control-address buses extend toward the corners of the square circumscribed by the memory devices . In the illustrated embodiments, the memory devices forming the pairs abut at their first ends, as shown in the Figures.

Discussion of the Cited References

Schumacher discloses a system in which integrated circuits (IC) are designed such that the pin assignments are substantially mirrored about an axis. The ICs are mounted to a circuit board such that one IC is rotated 180 degrees relative to another IC mounted some distance therefrom. Likewise, an IC may mount on an opposite side of the circuit board and

rotated 180 degrees from another IC. Schumacher teaches only integrated circuits arranged in rows, rather than surrounding a memory hub. Schumacher fails to teach that integrated circuits on the same side of the circuit board abut one another.

Schumacher teaches that this arrangement enables leads to be "routed in the same direction and less likely to have cross over problems." Col. 2, lns. 57-59. The teachings of Schumacher do not suggest modification of Ryan. As shown in Ryan (Figure 2 of Ryan is reproduced to the left), individual buses radiate outwardly from the memory hub and directly connect each memory device to the memory hub without crossing. There is therefore no possibility of crossover and no simplification would occur from using the arrangement of Schumacher. One skilled in the art would not see any use for using the arrangement of Schumacher with the device of Ryan – it would require rearrangement and reengineering without achieving the improvement claimed by Schumacher. It therefore would not be obvious to combine Schumacher and Ryan to achieve the disclosed embodiment.

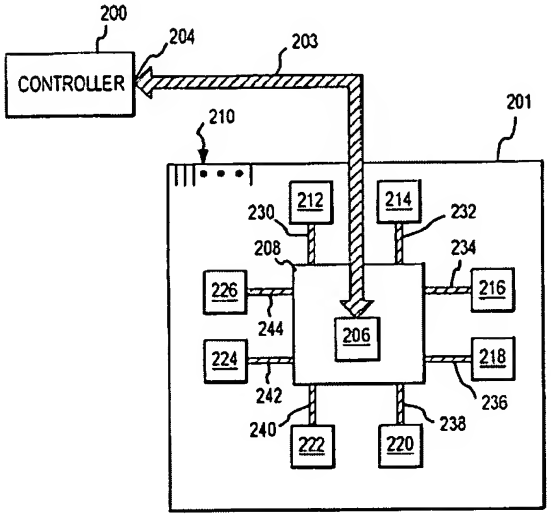

FIG.2

Discussion of the Claims

Turning now to the claims, the patentably distinct differences between the cited references and the claim language will be specifically pointed out.

With respect to claim 1, none of the cited references teach or suggest, in combination with the other limitations of claim 1, a memory module including "a plurality of memory devices positioned *around the memory hub* and arranged in pairs on the same side of the circuit board as one another, each memory device having the same physical pin layout and including pins associated with a first functional group of signals adjacent a first end of each memory device and pins associated with a second functional group of signals adjacent a second end of each memory device, *and the first end of each memory device in each pair being*

positioned adjacent one another on the circuit board and the second end of each device in a pair being positioned adjacent a second end of a device in one of the other pairs." (emphasis added).

With respect to claim 10, none of the cited references teach or suggest, in combination with the other limitations of the claim, a memory module having "a plurality of memory devices positioned *around the memory hub* and arranged in pairs on the same side of the circuit board as one another, each memory device having the same physical pin layout and including pins associated with a first functional group of signals adjacent a first end of each memory device and pins associated with a second functional group of signals adjacent a second end of each memory device, *and the first ends of each memory device in each pair being positioned substantially abutting* one another on the circuit board." (emphasis added).

With respect to claim 14, none of the cited references teach or suggest a memory module including "four pairs of devices, each pair being positioned *substantially perpendicular to adjacent pairs and located* adjacent a respective edge of the circuit board, and wherein the first functional group of signals comprise data signals and the second functional group of signals comprise control-address signals." (emphasis added).

With respect to claim 21, none of the cited references teach or suggest, in combination with the other limitations of the claim "a plurality of memory devices positioned around the memory hub and arranged in pairs on the same side of the circuit board as one another, each memory device having the same physical pin layout and including pins associated with a first functional group of signals adjacent a first end of each memory device and pins associated with a second functional group of signals adjacent a second end of each memory device, *and the first ends of each memory device in each pair substantially abutting one another on the circuit board*." (emphasis added).

With respect to claim 26, none of the cited references teach or suggest, in combination with the other limitations of the claim, a method including the step of "positioning pairs of memory devices around the memory hub such that both devices in each pair are on the same side of the circuit board and *each pair is substantially perpendicular to adjacent pairs, each memory device in a respective pair being physically rotated 180 degrees in the plane of the circuit board relative to the other device in the pair*." (emphasis added).

Claims 2-9, 11-13, 15-20, 22-25, and 27-30 are allowable as dependent on allowable claims 1, 10, 21, and 26, respectively.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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